IN THE SPECIFICATION

Please amend the Specification as follows.

[0008] Another advantage of using silicon nitride layer is that during the programming process the electrons are stored locally in the channel, close to the source side or the drain side. Hence, during the programming process, the voltage can be applied to the source region and the control gate in one end of the stacked gate, and the Gaussian-distributed electrons are ~~store~~ stored in the silicon nitride layer at the drain region in the other end of the stacked gate~~, and~~. The voltage can also be applied to the drain region and the control gate in one end of the stacked gate, and the Gaussian-distributed electrons are stored in the silicon nitride layer at the source region in the other end of the stacked gate. Therefore, by changing the voltages applied to the control gates and the above two regions, there may be two groups of Gaussian-distributed electrons, one group of Gaussian-distributed electrons, or no electrons in a single silicon nitride layer. Hence, the flash memory using a silicon nitride layer to replace the floating gate can be programmed in four states, and such a memory cell is a two bits in one cell flash memory cell.

[0025] FIGs. 1A-1G are cross-sectional views showing the progression of steps for fabricating a non-volatile memory in accordance with an embodiment of the present invention. Referring to FIG. 1A, a tunneling layer 102, a trapping layer 104 and barrier layer 106 are sequentially formed on a substrate 102. The material of the substrate 100 is, for example, silicon; the barrier layer 102 is, for example, a silicon oxide layer. The trapping layer 104 is, for example, a silicon nitride layer. The barrier layer 106 is, for example, a silicon oxide layer.

[0026] A polysilicon layer 108 and a metal silicide layer 107 are sequentially formed on the barrier layer 106, wherein the polysilicon layer 108 and the metal silicide layer 107 form a gate conductive layer 105. An anti-reflection layer 110 is formed on the gate conductive layer 105. Wherein, the polysilicon layer 108 is formed by a method including, for example, a chemical vapor deposition. The metal silicide layer is formed by a method including, for example, forming a metal layer on the polysilicon layer 108, and performing a thermal process to cause a reaction between the metal layer and the polysilicon layer 108, so as to form the metal silicide layer 107. A photoresist layer 112 with a pattern is formed ~~a~~ on the anti-reflection layer 110 by the photolithographic processes.

[0028] In the foregoing photolithographic process on the photoresist layer, the anti-reflection layer 110 can absorb light, so that the exposing light source is prevented from an interference between the incident light and the reflected light from the substrate or the film layer. Also and, the anti-reflection layer 110 includes, for example, organic or inorganic dielectric materials. If the anti-reflection layer 110 includes the inorganic dielectric material, the fabrication processes are ~~following~~ described as follows.

[0029] In FIG. 1C, after the photoresist layer 112 is removed, since the anti-reflection layer 110a includes the inorganic dielectric material, the anti-reflection layer 110a is not removed while removing photoresist layer 112. Then, ~~then~~ the exposed surface of the control gate 105a, that is, the surface at the sidewalls of the control gate 105a, is formed with a thin oxide layer 119. In one embodiment, the thin oxide layer 119 is formed, for example, by a thermal oxidation process,

wherein the oxygen and nitrogen gases are flowed through. Here, the thin oxide layer 119 and the anti-reflection layer 110a can be used to protect the control gate 105a form being damaged by the subsequent fabrication process.

[0031] Referring to FIG. 1E, a plasma enhanced CVD (PECVD) is performed to form an ultraviolet-resistant lining layer 118 on the surfaces of the substrate 100 and the spacer 116. In a preferred embodiment of the present invention, the material of the ultraviolet-resistant lining layer 118 is silicon nitride, for example. The process parameters for forming the ultraviolet-resistant lining layer 118 are as follows. The reacting gas includes a silane (SiH_4) gas with a flow rate between 50sccm and 60sccm, preferably 55sccm, an ~~ammonium~~ ammonia (NH_3) gas with a flow rate between 20sccm and 30sccm, preferably 25sccm, and a nitrogen (N_2) gas with a flow rate between 2600sccm and 3000sccm, preferably 2800sccm. The temperature for the PECVD process is between 380°C and 420°C, preferably 400°C; the power for the PECVD process is between 370W and 410W, preferably 390W; the pressure for the PECVD process is between 7.0 torr and 8.0 torr, preferably 7.5 torr. The thickness of the film is between 180Å and 220Å, preferably 200Å. It should be noted that the flow rates of SiH_4 and NH_3 and the applied power are smaller than those in the conventional method. Hence, the thin film formed under those parameters is much denser because of a lower deposition rate.

[0037] In addition, in another embodiment of the invention, the anti-reflection layer 110a is formed ~~form~~ from an organic material. In this manner, after the stacked structure 113 (such as FIG. 1B) is patterned, the photoresist layer

is removed to expose the control gate 105a, as shown in FIG. 2A. Here, since the anti-reflection layer is formed by organic material, during removing the photoresist layer 112, the anti-reflection layer 110a is removed at the same time. Then, the exposed surface of the control gate 105a is formed with a thin oxide layer 119a, wherein the thin oxide layer is formed, for example, on top and side walls of the control gate 105a. The thin oxide layer 119a is used to protect the control gate 105a from being damaged from subsequent fabrication processes. The thin oxide layer 119a is similar to the thin oxide layer 119 in material and fabrication method.